Effect of Chemical and Processing Parameters on Hole Filling Characteristics of Copper Electroplating

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Abstract

Miniaturization and increased functionality demands of electronics have substantially decreased the sizes of electronic features that need to be plated. The circuit density of printed circuit designs has been increasing accordingly. Copper is the most preferable metal used in electronic industry for filling small features due to its electrical and thermal conductivity properties and the possibility of electroplating. New technologies started to develop in order to completely fill through vias in build-up core layers in HDI and IC with solid copper. This has been associated with improved thermal and mechanical properties as well as with increased reliability. In this paper the effect of the chemical composition and the processing parameters on the hole filling characteristics of copper electroplating has been studied. It was established that a preliminary treatment in a chemical solution was the most significant factor for void free filling of blind micro vias. Copper concentration was also significant factor, while the leveler concentration was only significant in some cases. The brightener concentration was not a significant factor for the responses tested, which included the fill ratio, dimple, planarization, and surface copper thickness. The optimum conditions of a DC process for filling up a wide range of via sizes and plating simultaneously though holes were determined. The results obtained allow for enhancing via plating capabilities and increasing the reliability. The second part of this paper shows a novel process for filling through vias in core layers up to 400 mkm thick. This process includes two subsequent steps, being PPR or DC plating depending on the substrate thickness and hole diameters. The through vias were completely filled by using a modified process for acid copper electroplating. The chemical and plating parameters are discussed in the paper. Data enclosed demonstrate through vias in build-up core filled without any voids and defects. This innovative technology is at an early stage being at the process of further optimization to enable a variety of HDI and IC substrate package designs.

Introduction

Miniaturization and increased functionality demands have substantially decreased the sizes of electronic features that need to be plated. Copper is the most preferable metal used in electronic industry for filling small features due to its electrical and thermal conductivity properties and the possibility of electroplating. Vias that are not filled can lead to solder voids and reduced reliability. The conventional copper filling technologies are not capable of plating through holes at the same time as filling vias due to the reliability problems. Micro-vias filling by copper electroplating is an important technology in the fabrication of high density interconnections (HDI) of printed circuit board (PCBs) and IC package substrates [1-3]. New technologies started to develop in order to completely fill through vias in build-up core layers in HDI and IC with solid copper. This has been associated with improved thermal and mechanical properties as well as with increased reliability.

In this paper the effect of the chemical composition and the processing parameters on blind via filling characteristics of copper electroplating has been studied. The optimum conditions for filling up a wide range of via sizes are determined. The results obtained allow for enhancing via plating capabilities and increasing the reliability. The second part of this paper shows a novel process for filling through vias in core layers. Data enclosed demonstrate through vias in build-up core filled without any voids and defects.

Acid Copper Plating Process

A typical copper plating solution contains copper sulfate, sulfuric acid, chloride ions, and organic additives that control the deposition process and the quality of the plated coatings [4-6]. Various organic compounds are used in plating baths during the production of PCBs, chip carriers, and semiconductors [7, 8]. They act as levelers and brighteners enabling as uniform a deposition of copper as possible on different regions of the PCB including through holes and BMVs. The purpose of this work was to determine the effect of the organic additive species, their concentration as well as the processing parameters on via filling. In general there are three basic additives that are used in acid copper electroplating baths: Wetter, Brightener, and Leveler. The Wetter (suppressors, high molecular weight polyether compounds and polyoxyalkylene glycols) in the presence of chloride ion has a strong polarizing influence producing a large decrease in the exchange current density. Addition of Brightener such as sulfopropyl sulfides to an acid copper electrolyte acts as a depolarizer producing an increase in exchange current density. As an example, the maximum depolarization effect for SPS (disodium bis (sulfopropyl) disulfide) was observed at a concentration of 5 ppm. Above this concentration of the brightener, the surface blocking effect of the adsorbed brightener mitigates the depolarizing effect to some degree. The brightener spices are much smaller molecules than the wetter molecules and so the adsorption of the wetter does not appear to significantly interfere with the adsorption of the brightener. Leveler adsorbs preferentially near the most negatively charged sites of the cathode (PCB), thus slowing down the plating rate at high current density areas. The organic additives affect the secondary current distribution and control the physical mechanical properties of the metal deposits considerably important being tensile strength and elongation.

Blind Micovia Filling

Test Vehicles

The tests vehicles included various via diameters in 4" x 4" grid, Figure1. Side 1: vias 75 microns deep; via diameter 75, 100, 125, and 150 microns. Side 2: vias 100 microns deep, via diameter 100, 125, 150, and 175 microns; glass re-enforced dielectric. Through holes were interspersed with the grid. All via geometries were plated simultaneously.

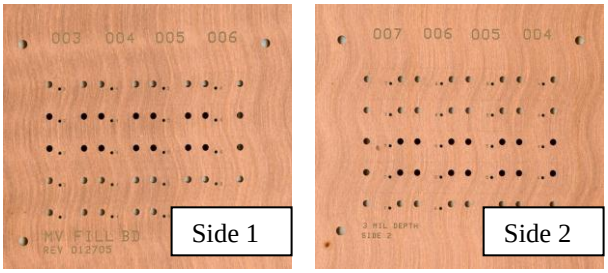


Figure 1 – Test Vehicles

Surface Copper Thickness and Via Fill Criteria

Figure 2 shows the surface copper thickness measurement. The Fill Ratio is defined as the ratio B/A in percents, Figure 3. Fill Ratio = B/A x100. The acceptable value of the Fill Ratio is 80% or higher.

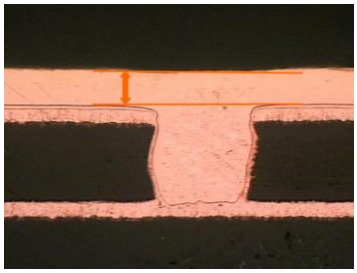


Figure 2 – Surface Copper Thickness

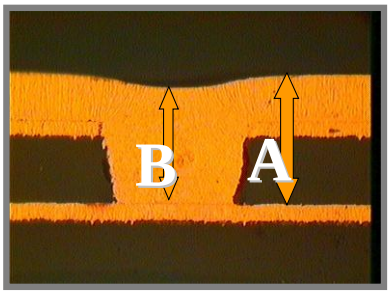


Figure 3 – Fill Ratio

DOE

Experiment was designed (DOE) that included runs with various concentration levels of electroplating solution constituents and various plating conditions. MacDermid MacuSpec VF organic additives were used. A DC plating regime was explored. Four factors were studied: copper ions concentration, brightener and leveler amounts in the bath, and preliminary treatment of the test vehicles in a pre-dip bath. Four concentration levels of the bath constituents were included. The pre-dip was a categorical factor – two levels – "yes" – included in the process flow or "no" – not included. The responses measured were the Fill Ratio, dimple depth, inclusions (voids) for various sizes diameter vias and the surface copper thickness. The goal was to minimize the thickness of copper deposited on the surface, to minimize the dimple depth, to eliminate voids (void free filling) and to obtained an optimum Fill Ratio of 80% or higher. Thus enhancing via filling capabilities of the process could be achieved. The results obtained are shown in the Figure 4 to Figure 10.

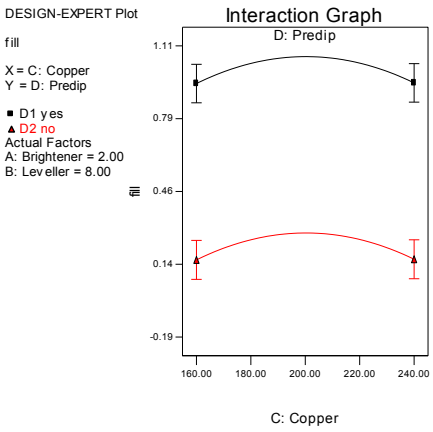


Figure 4 – Fill Ratio as a Function of Copper Sulfate Concentration, g/l and Pre-dip for 75 x 75 μm vias. Brightener 2 ml/l, Leveler 8ml/l

A similar graph as shown in Figure 4 for the Fill Ratio as a function of copper concentration and the pre-dip but at 8 ml/l brightener concentration in the bath shows the same trend. The values of the Fill Ratio are very close to the values obtained at the lowest brightener concentration, 2 ml/l, shown above. At usually used brightener concentration 6 ml/l the measurements were similar as well. This showed that the brightener concentration in the plating bath did not affect significantly via filling process.

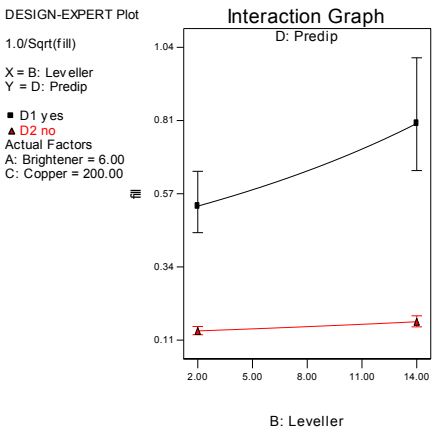


Figure 5 – Fill Ratio as a Function of Leveler Concentration, ml/l and Pre-dip for 100 x 100 µm vias. Brightener 6 ml/l, Copper Sulfate 200 g/l

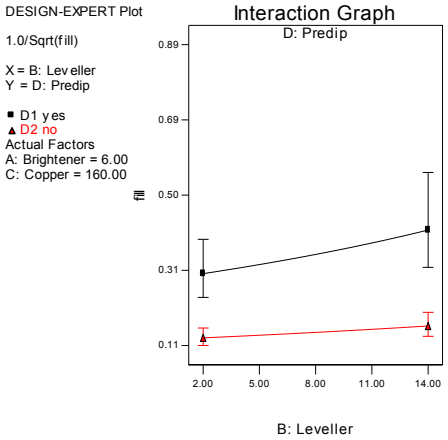


Figure 6 – Fill Ratio as a Function of Leveler Concentration, ml/l and Pre-dip for 125 x 100 µm vias. Brightener 6 ml/l, Copper Sulfate 160 g/l

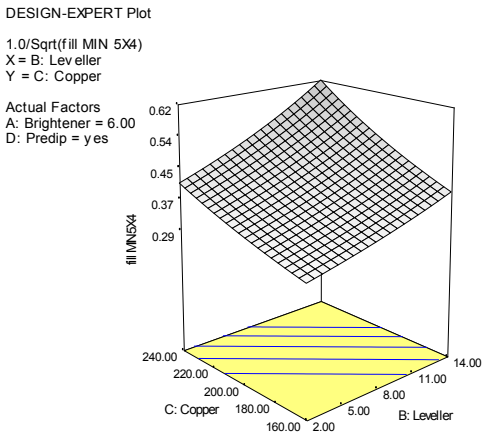


Figure 7 – Fill Ratio as a Function of Copper Sulfate Concentration, g/l and Leveler Concentration, ml/l for 125 x 100 µm vias. Brightener 6 ml/l

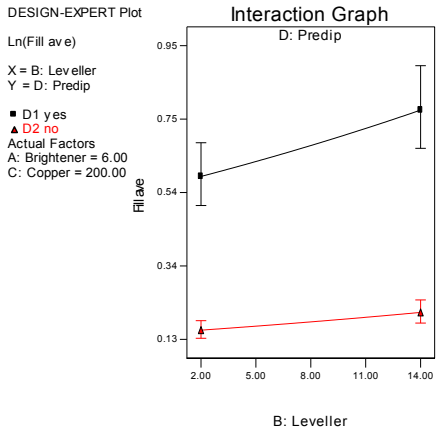


Figure 8 – Overall Average Fill Ratio as a Function of Leveler Concentration, ml/l and Pre-dip. Brightener 6 ml/l, Copper Sulfate 200 g/l

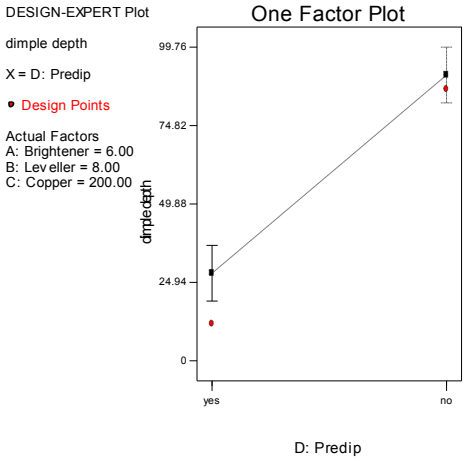


Figure 9 – Dimple Depth for 100 x 100 μm vias as a Function of the Pre-dip. Brightener 6 ml/l, Leveler 8 ml/l, and Copper Sulfate 200 g/l

The factors that were significant for filling vias were determined as a result of this study. The most significant factor was the use of Pre-dip. It reduced the dimple depth and increased the Fill Ratio considerably. Leveler concentration was found to be sometimes significant for filling vias. The optimization gave a recommended concentration of 14 ml/l for achieving high Fill Ratio and void free filling. Copper sulfate concentration was also found to be significant, the higher being the better. The recommended concentration was 240 g/l. Particularly important was found to be the interaction between the bath constituents and the process sequence. Surface copper thickness decreased as the leveler concentration increased form 2 to 14 ml/l with the pre-dip used. The brightener concentration was found not to be significant for the responses tested. The results from these experiments allowed optimizing the electroplating bath chemistry and the process sequence for filling up vias and minimizing the surface copper thickness. The trough holes were plated as a part of this study to measure the physical mechanical properties and thermal performance of plated copper. The measured Tensile Strength of 41,000 – 42,000 psi and Elongation of 19 – 22% met the IPC specification. The reliability was evaluated by performing solder shock resistance measurements at 280 C for 10 seconds float, IPC 2.6.8. No cracks were observed after 6x solder shock.

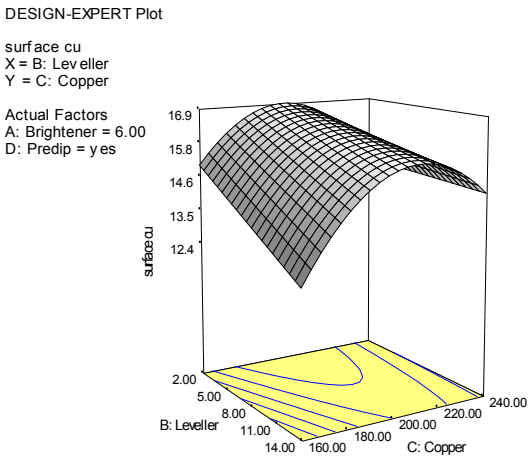
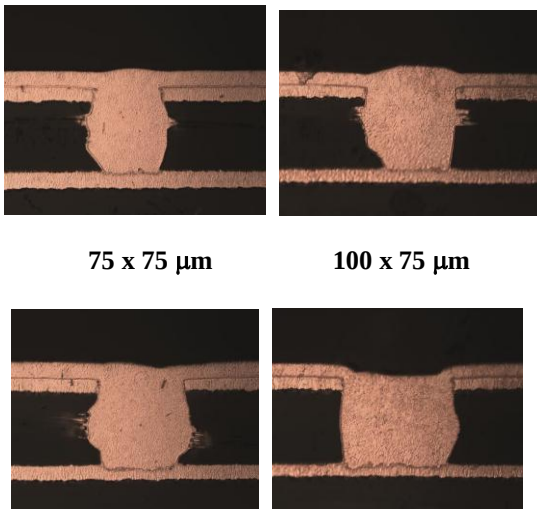


Figure 10 – Surface Copper Thickness in microns as a Function of Leveler concentration, ml/l and Copper Sulfate concentration, g/l with Pre-dip. Brightener 6 ml/l

Cross section pictures shown in Figure 11 demonstrate various sizes vias filled at optimum plating conditions.



75 x 75 µm **100 x 75 µm**

100 x 100 µm **125 x 100 µm**

Figure 11 – Copper Sulfate 240 g/l, Leveler 8 ml/l, Brightener 2 ml/l

Through Via Fill for HDI and IC Substrates

The results from the above study were used further in developing a new process for filling through micro vias. Filling through via holes by copper electroplating started to develop recently to benefit the fabrication of printed circuit boards (PCBs) with high-density interconnections (HDI) [9] and three dimensional (3D) chip stacking [10]. For the latest package substrates designs electrodeposited copper is already being used to fill through vias. Through vias filled with copper has the advantage over any type of resin material available, due to copper thermal and electrical characteristics being significantly better. Using copper through via filling process could reduce the overall cost of package substrate production. There are differences between the plating processes for filling blind micro-vias and through vias due to the differences in the geometric shapes. The differences include the hydrodynamic conditions, solution flow in and out of the through vias. Copper could be deposited in a center-up mechanism, as opposite to the bottom up mechanism in case of blind micro vias. In this study results from utilizing a new process for filling up through vias are demonstrated. Various plating regimes

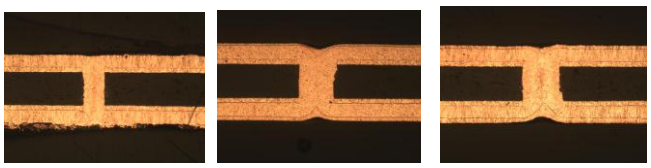
were used, including DC plating, Pulse Reverse Plating, and combination between them. The final plating results depended on the bath chemistry as well as on the plating parameters.

Test Vehicles for Filing Through Vias

The test vehicles used for through vias fill were 0.15 mm and 0.40 mm thick boards. Via diameters were 75, 100, 125, 150 and 200 microns. In addition to these tests vehicles, flexible substrates were plated. The thickness of the substrate was 50 microns and the hole diameters were 50 and 100 microns.

Plating Results

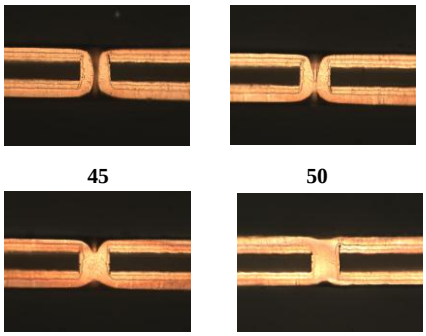
The cross section coupons were taken from the plated boards. Figure 12 shows filled through vias, 75, 100, and 125 microns diameter in 150 microns thick test vehicles.



3 mils **4 mils** **5 mils**

Figure 12 – Through Hole Fill of 75, 100, and 125 μm diameter x 150 μm thick

The cross sectional shape of copper deposited within the through vias during the plating process is shown in Figure 13. The deposition rate on the hole walls, hole corners and on the surface depends on the plating conditions. In the case of plating shown below, this rate was higher in the center of the hole at the earlier stages of the plating. As the plating process continued further, the top and the bottom parts of the hole were filled up void free.



45 **50**

60 **70**

Figure 13 – Through Hole Fill as a Function of Time, minutes. DC regime

The efforts were directed toward reducing the surface copper thickness. Figure 14 shows 50 microns filled through vias in 50 microns thick substrate with 15 microns copper plated on the surface, DC plating regime.

Figure 14 – Through Hole Fill, 50 μm diameter in 50 μm thick flexible substrate

A two step process using two acid copper plating electrolytes was utilized for filling through holes in thick tests vehicles. Through holes 200 microns diameters in 400 microns thick tests vehicles could be filled with solid copper, Figure 15.

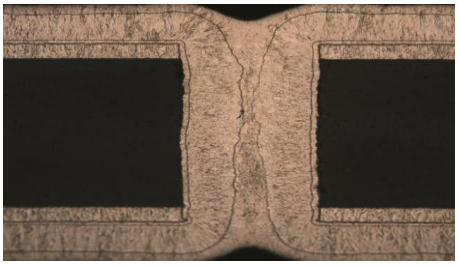


Figure 15 – Filing 200 μm through holes in 400 μm thick substrate

This innovative technology is at an early stage. It is at the process of further adjustments, chemistry and current regimes optimization to enable a variety of HDI and IC substrate package designs.

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Filling Small Features

- Miniaturization and increased functionality demands of electronics have substantially decreased the sizes of electronic features that need to be plated.

- Copper is the most preferable metal used in electronic industry for filling small features
  - Electrical conductivity
  - Thermal conductivity properties
  - Possibility of electroplating

Use of Electroplated Copper to Fill Microvias

Benefits

- Electro-deposition of copper has been the interconnection technology for the PCB fabrication for fifty years.
- Copper-filled micro-vias are more conductive than conductive paste filled micro-vias.
- Copper-filled micro-vias easily and reliably enable the use of stacked via designs. Stacking allows higher circuit densities and better thermal management.
- Copper-filled vias improve thermal conductivity and heat dissipation in PWBs.

MicroVia Filling

- Via in pad BGA designs that are not filled can lead to solder voids which negatively affect reliability
- Goal:
  - Optimizing the acid copper plating process to enhance via plating capabilities and increase the reliability
- Plating through holes at the same time as filling vias

Through Via Fill

- Micro-vias filling by copper electroplating is an important technology in the fabrication of high density interconnections (HDI) of printed circuit board (PCBs) and IC package substrates

- Need for better performance, miniaturization, and price reduction of portable electronics

- Development of new technologies for completely fill through vias in build-up core layers in HDI and IC with solid copper

Copper Electroplating Process

Filling characteristics of copper electroplating

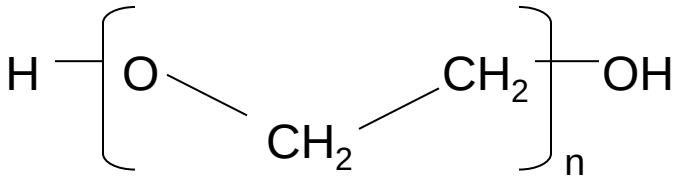
- Effect of:
  - Chemical composition of copper electrolytes
    Plating components
  - Processing parameters
- Responses, BMV:
  - Fill Ratio
  - Dimple Depth
  - Surface Copper Thickness
  - Voids Formation

Plating Components Inorganic

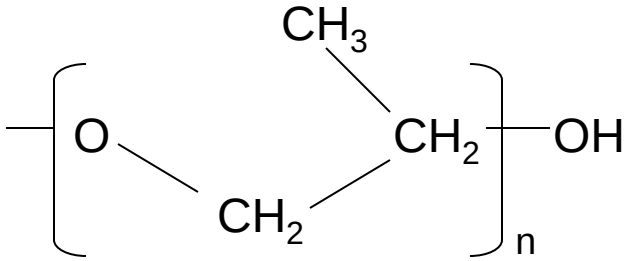
- Sulfuric acid - Principal function is to provide conductivity of the solution
- Copper sulfate – The source of copper ions that are plated out onto the cathode
- Chloride – Enhances the adsorption and inhibition effect of the wetter. Chloride ions act as binding sites for the polyglycols. They assist in the corrosion of the copper phosphorous anode

Plating Components Organic

- Wetter (suppressor)– High molecular weight (polyglycols) suppressing agents that form a complex with chloride and are adsorbed onto the cathode forming a layer that inhibit transfer of brightener and leveler. They increase activation energy and slow the plating rate.



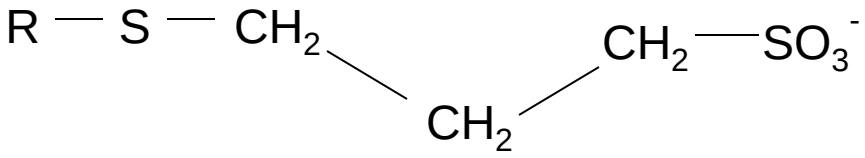
Polyethylene Glycol



Polypropylene Glycol

Plating Components Organic

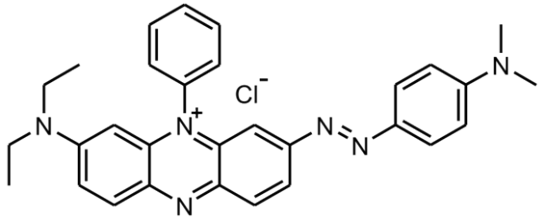
- Brightener (anti-suppressor)–Organic compounds that contain sulfur and other functional groups that are responsible for grain refinement. Increases rate of nucleation versus build up of existing nuclei. Brighteners lower activation energy and allow increased plating rate.



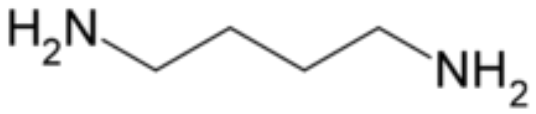
Brightener compounds

Plating Components Organic

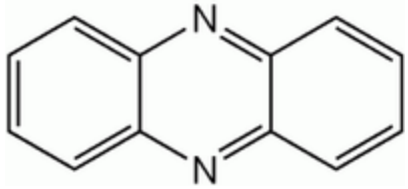
- Leveler - Organic compounds that are selectively adsorbed on readily accessible surfaces such as flat and protruding high points. They act as secondary suppressors and decrease plating rate.



Dyes

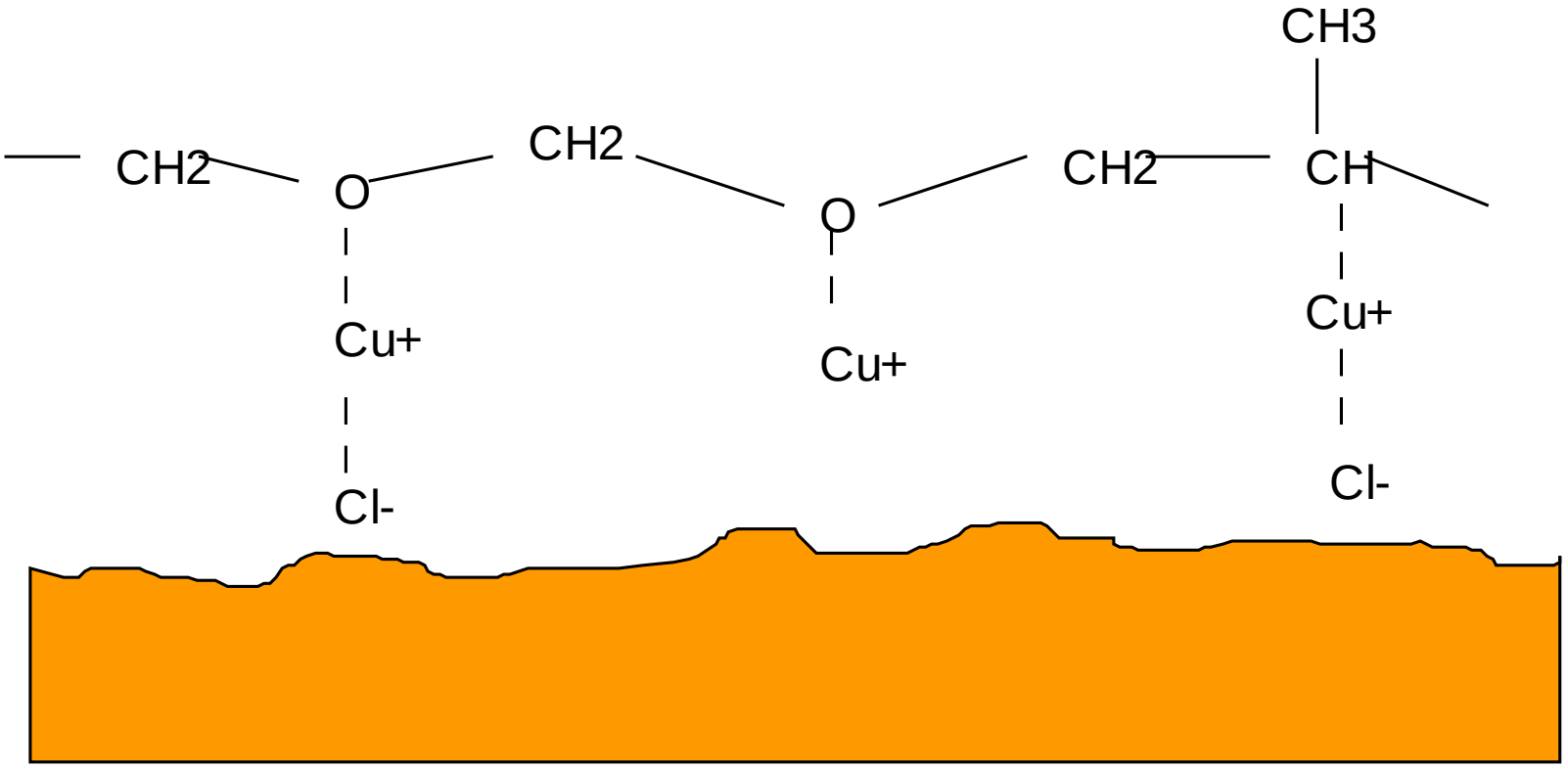


Polyamines

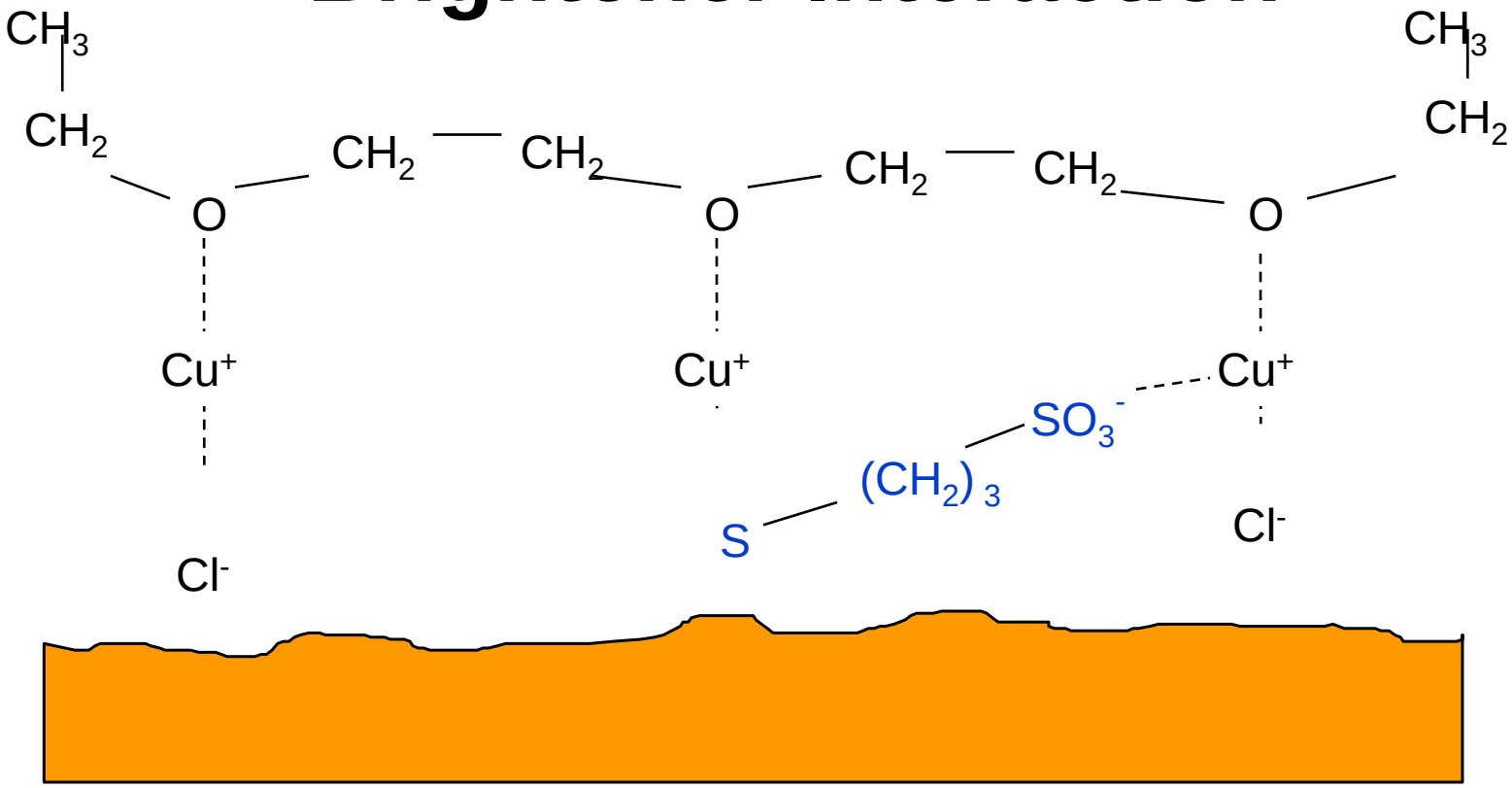


Aromatic Amines

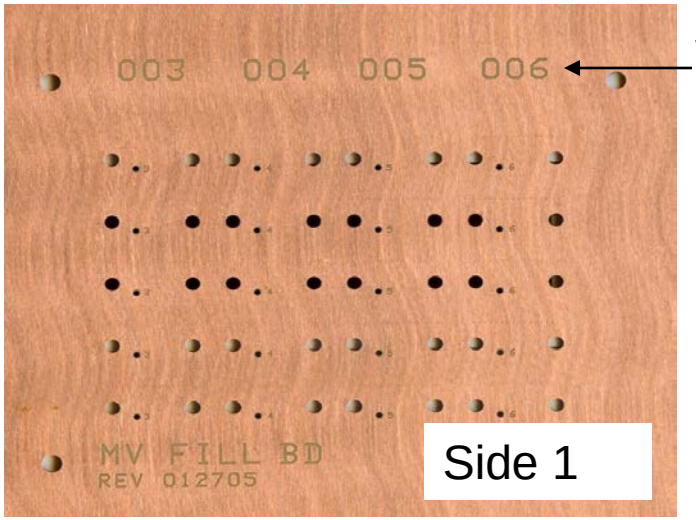
Wetter Interaction



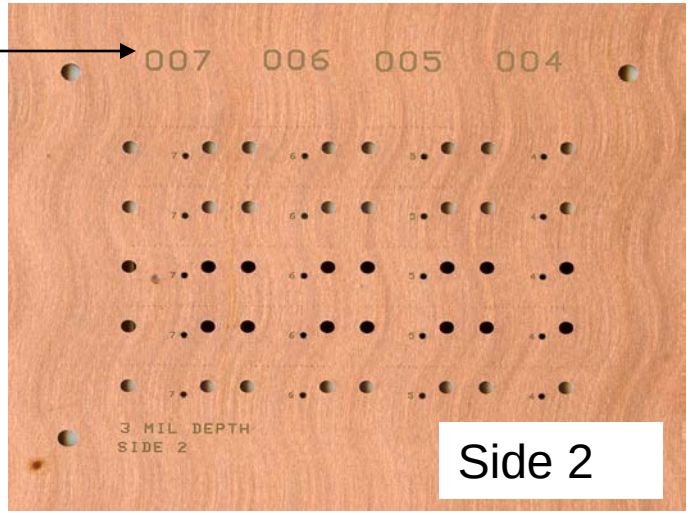
Brightener Interaction



Capability Test Vehicle



Via diameters



- Various via diameters in 4” x 4” grid. Simultaneously plating of all geometries
- Side 1: vias 3 mil deep; Side 2: vias 4 mil deep glass re-enforced dielectric
- Through Holes interspersed with the grid

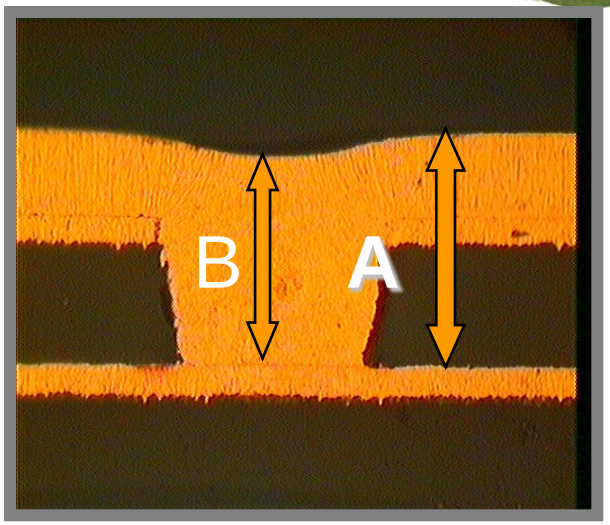
Metrics

Via Filling Criteria

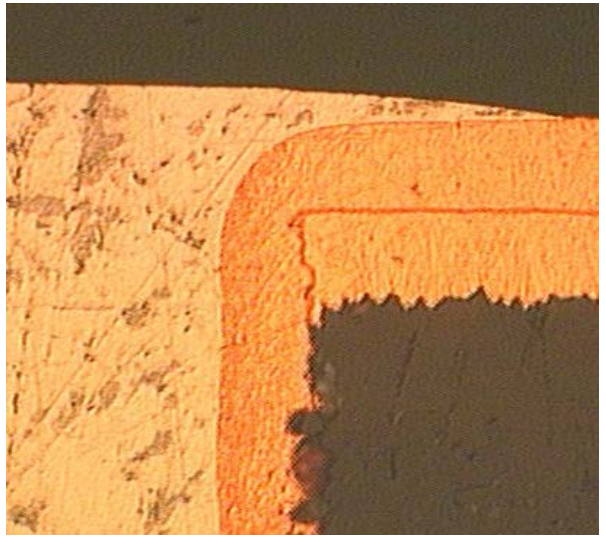
Fill Ratio = B/A **X** 100%

Acceptable > 80%

Minimize the amount of copper deposited on the surface of the PWB



Via filling capabilities across a wide range of geometry utilized in production of multilayer boards



Meet thermal reliability criteria (IPC 2.6.8)

6x Solder Shock

288°C for 10 seconds float

Tensile and Elongation that meet IPC spec

Process Flow

Acid Cleaner

Rinse

Microetch

Rinse

Acid Dip

Copper Via Fill Bath

- Cleaner wets the holes and removes light soils
- Etch undercuts any remaining debris
- Acidifies copper surface
- Electrolytic VF copper process

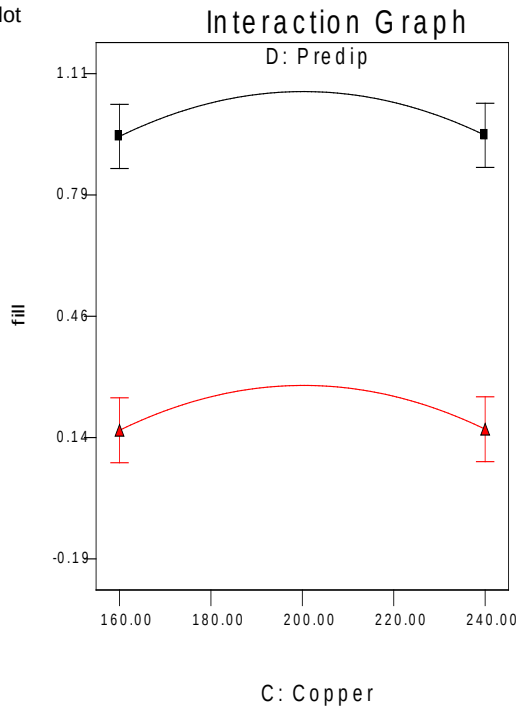
Results

DESIGN-EXPERT Plot

fill

X = C: Copper
Y = D: Predip

■ D1 yes
▲ D2 no
Actual Factors
A: Brightener = 2.00
B: Leveller = 8.00

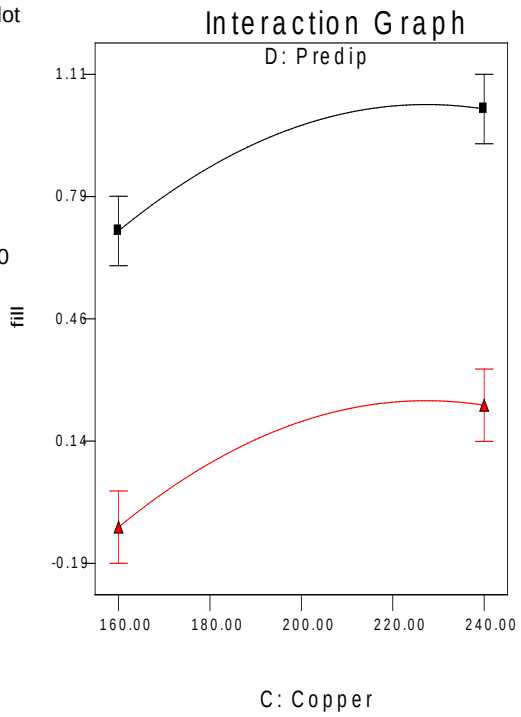


DESIGN-EXPERT Plot

fill

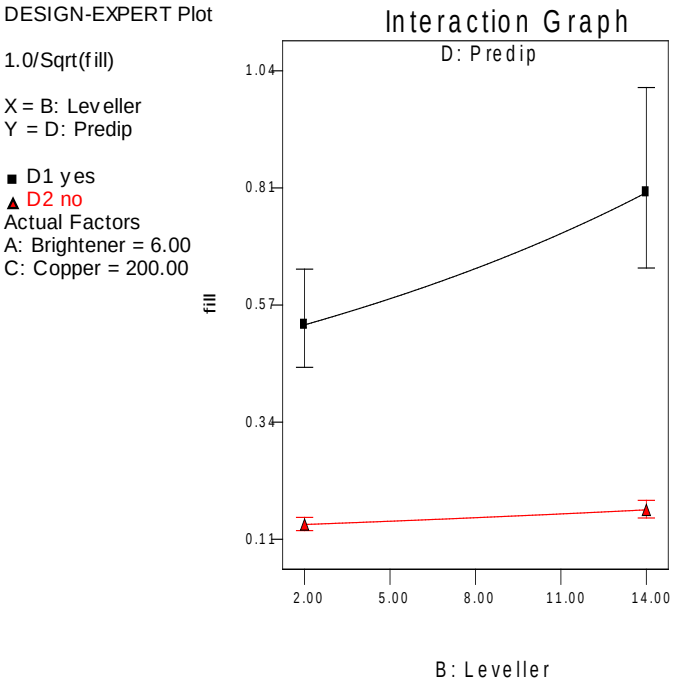
X = C: Copper
Y = D: Predip

■ D1 yes
▲ D2 no
Actual Factors
A: Brightener = 10.00
B: Leveller = 8.00



Fill Ratio 75 x 75 μm vias

Results



Fill Ratio
100 x 100 μm vias

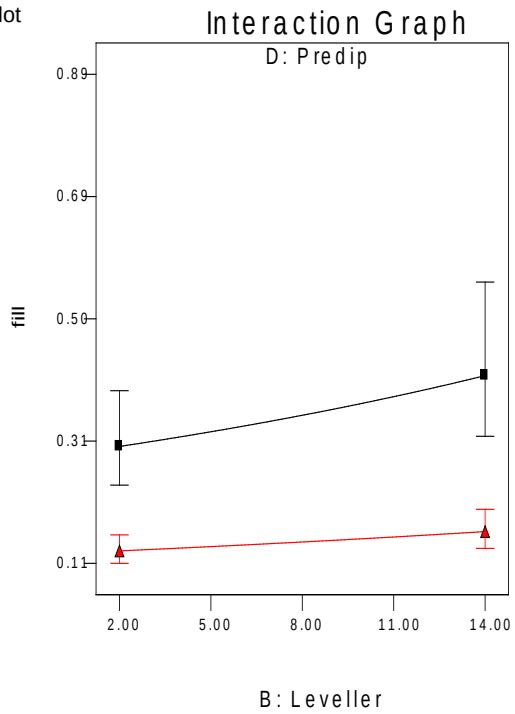
Results

DESIGN-EXPERT Plot

1.0/Sqrt(fill)

X = B: Leveller
Y = D: Predip

■ D1 yes
▲ D2 no
Actual Factors
A: Brightener = 6.00
C: Copper = 160.00

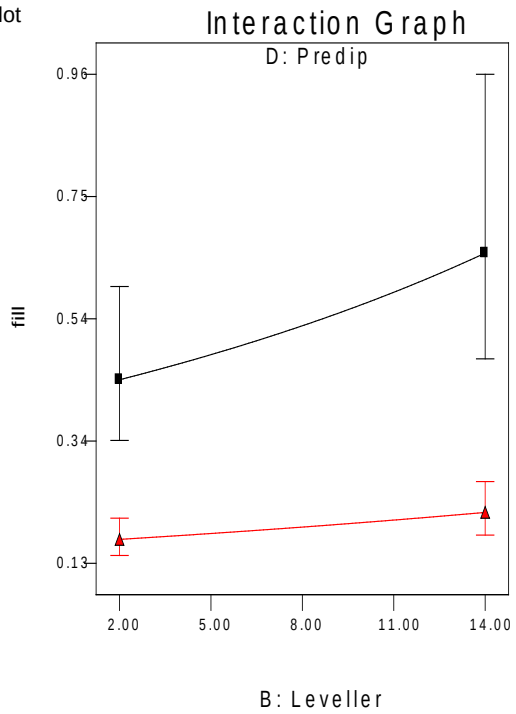


DESIGN-EXPERT Plot

1.0/Sqrt(fill)

X = B: Leveller
Y = D: Predip

■ D1 yes
▲ D2 no
Actual Factors
A: Brightener = 6.00
C: Copper = 240.00



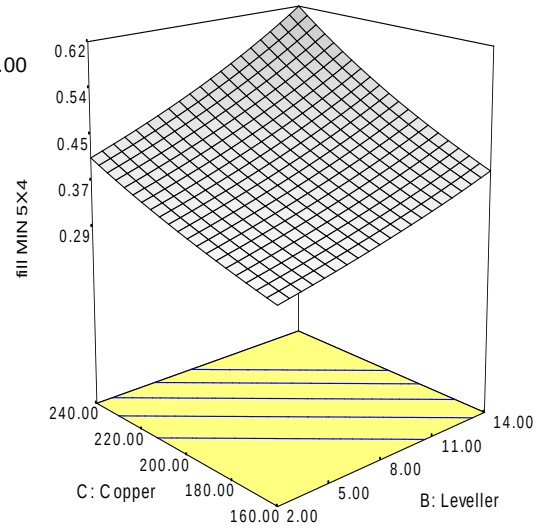
Fill Ratio 125 x 100 μm vias

Results

DESIGN-EXPERT Plot

1.0/Sqrt(fill MIN 5X4)
X = B: Leveller
Y = C: Copper

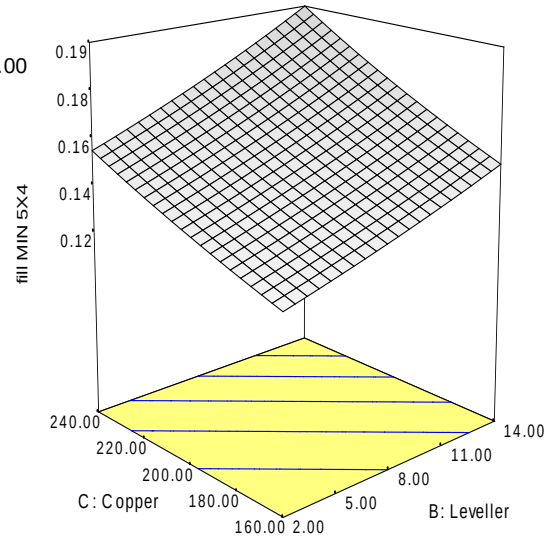
Actual Factors
A: Brightener = 6.00
D: Predip = yes



DESIGN-EXPERT Plot

1.0/Sqrt(fill MIN 5X4)
X = B: Leveller
Y = C: Copper

Actual Factors
A: Brightener = 6.00
D: Predip = no



125 x 100 μm vias

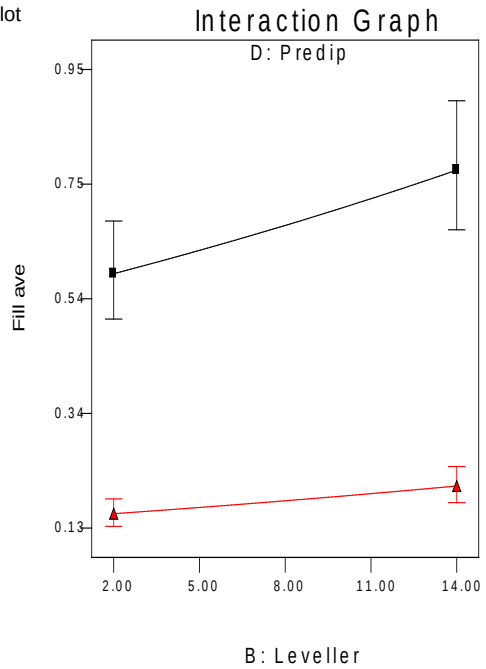
Overall Fill

DESIGN-EXPERT Plot

Ln(Fill ave)

X = B: Leveller
Y = D: Predip

■ D1 yes
▲ D2 no
Actual Factors
A: Brightener = 6.00
C: Copper = 200.00

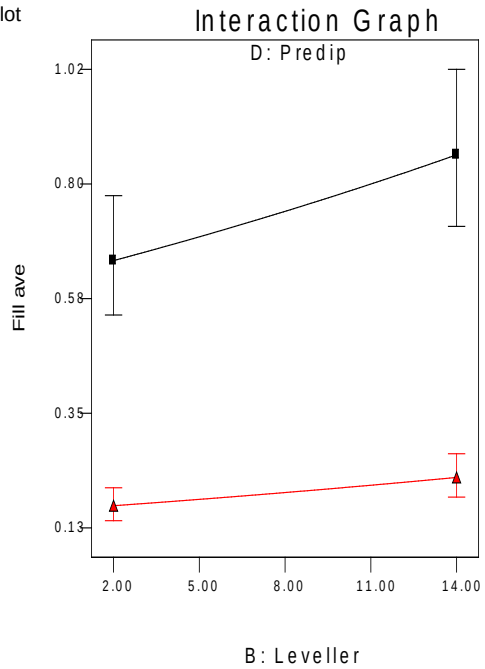


DESIGN-EXPERT Plot

Ln(Fill ave)

X = B: Leveller
Y = D: Predip

■ D1 yes
▲ D2 no
Actual Factors
A: Brightener = 6.00
C: Copper = 240.00



Dimple Depth

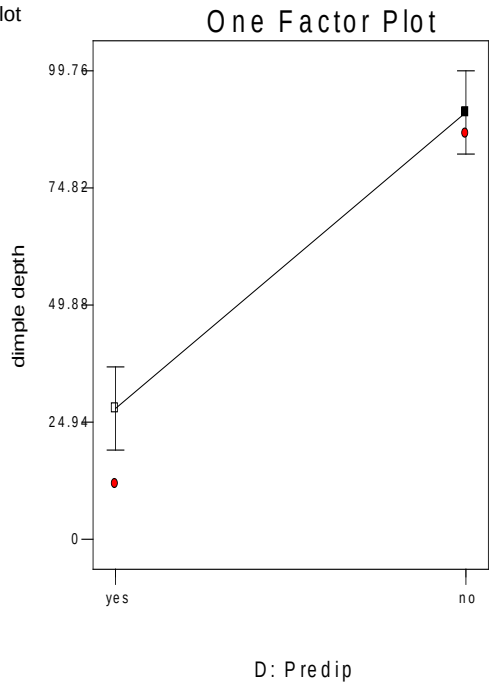
DESIGN-EXPERT Plot

dimple depth

X = D: Predip

Design Points

Actual Factors
A: Brightener = 6.00
B: Leveller = 8.00
C: Copper = 200.00



100 x 100 μm vias

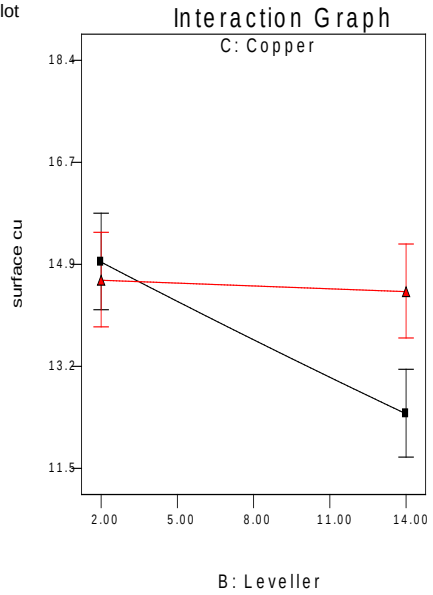
Surface Copper Thickness

DESIGN-EXPERT Plot

Sqrt(surface cu)

X = B: Leveller
Y = C: Copper

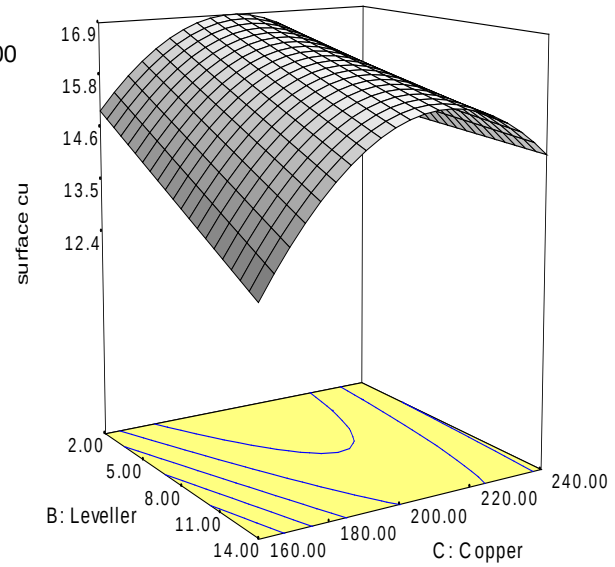
■ C- 160.000
▲ C+ 240.000
Actual Factors
A: Brightener = 6.00
D: Predip = yes



DESIGN-EXPERT Plot

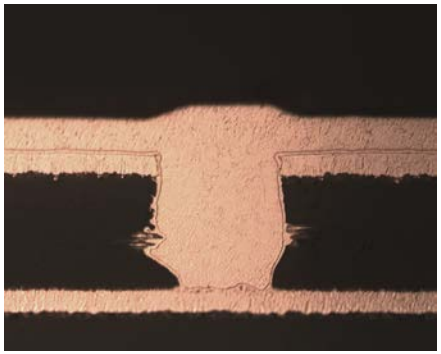
surface cu
X = B: Leveller
Y = C: Copper

Actual Factors
A: Brightener = 6.00
D: Predip = yes

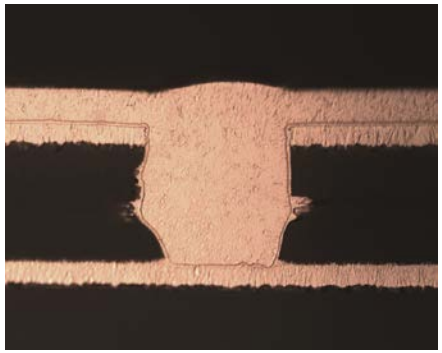


75 x 75 μm vias

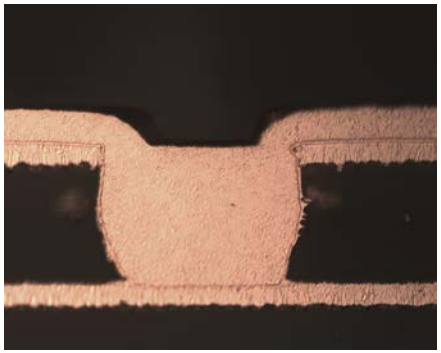
Cross Sections



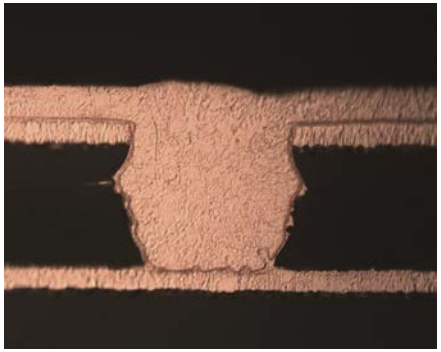
3 x 3



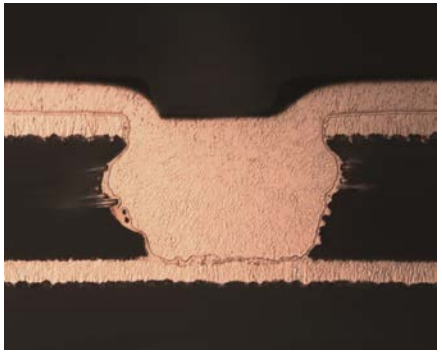
4 x 3



5 x 3



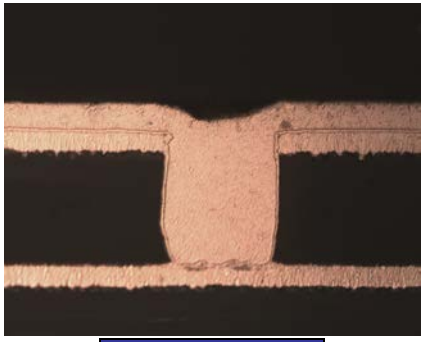
4 x 4



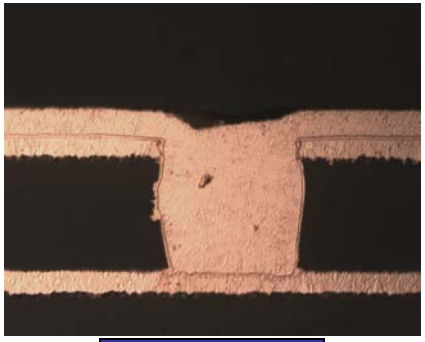
5 x 4

$CuSO_4x5H_2O$ 200 g/L, Leveler 2 ml/l, Brightener 10 ml/l

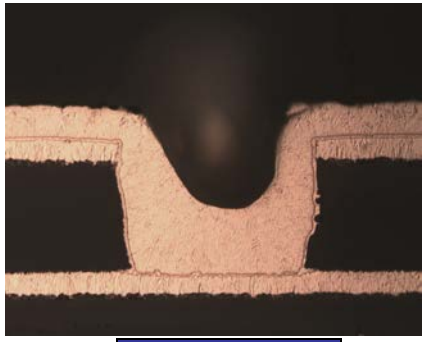
Cross Sections



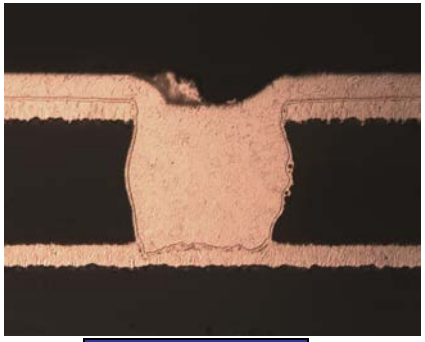
3 x 3



4 x 3



5 x 3

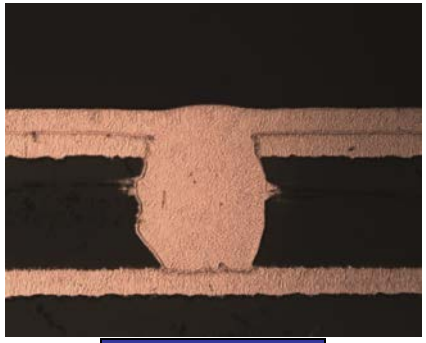


4 x 4

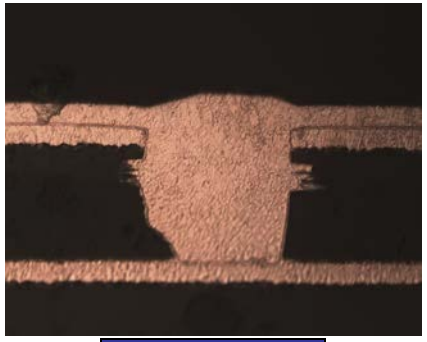
5 x 4

$CuSO_4x5H_2O$ 160 g/L, Leveler 14 ml/l, Brightener 2 ml/l

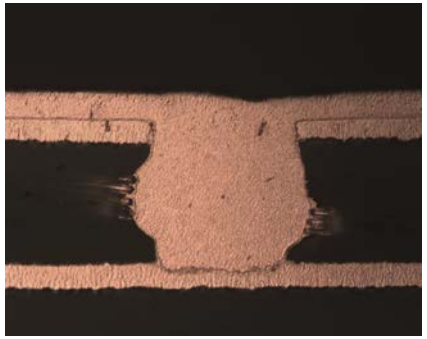
Cross Sections



3 x 3



4 x 3

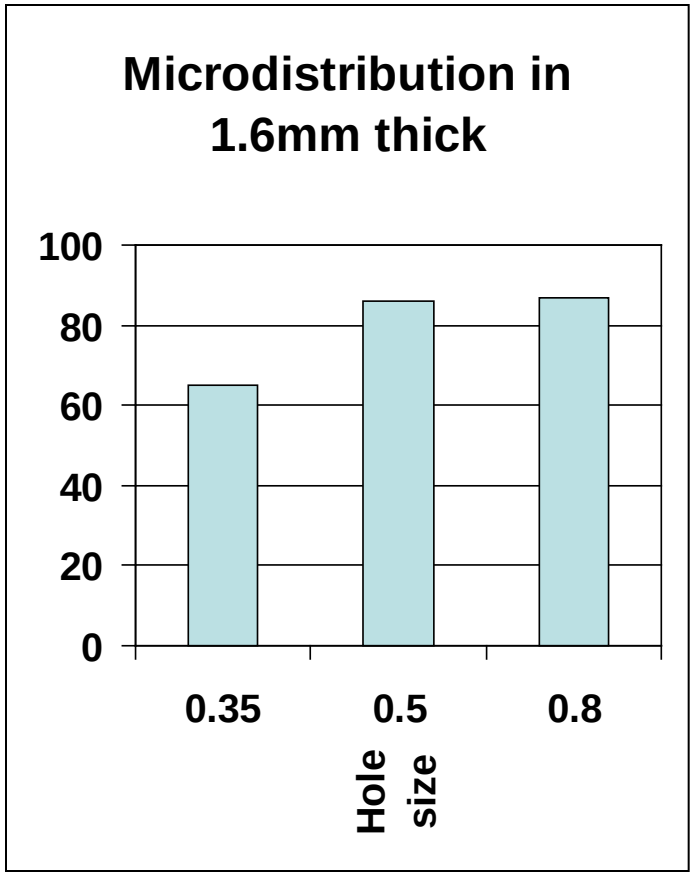


4 x 4

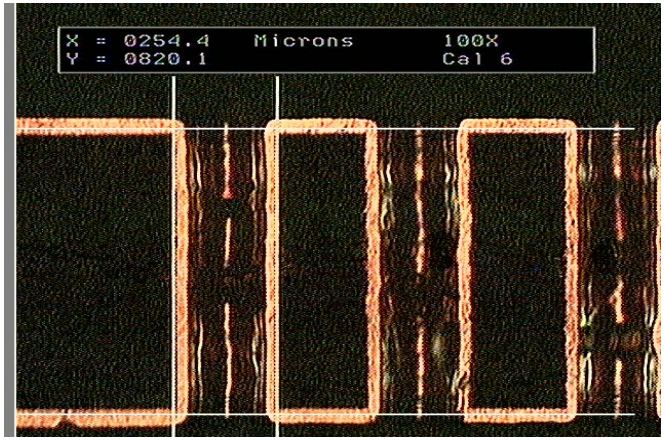
5 x 4

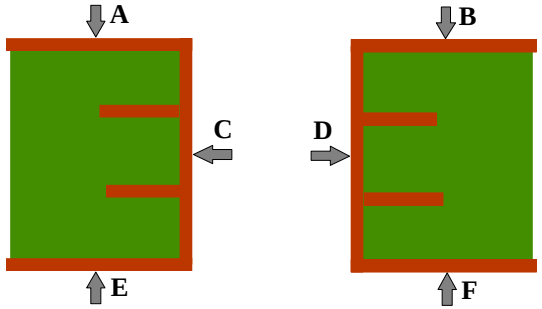
$CuSO_4x5H_2O$ 240 g/L, Leveler 8 ml/l, Brightener 2 ml/l

Throwing Power



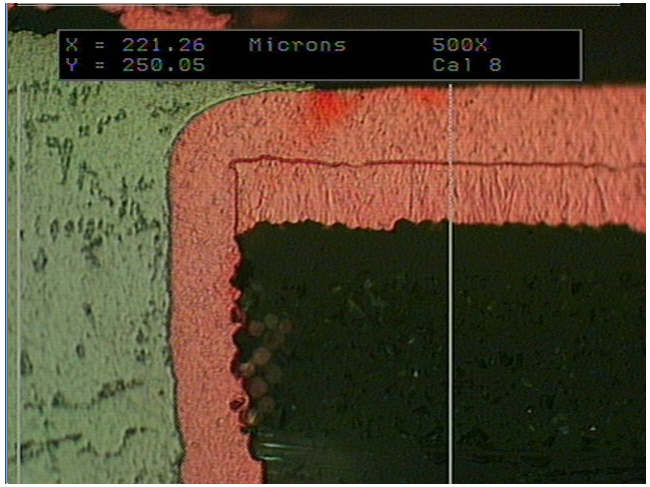
1.6mm thick panel





Microdistribution = [(C+D)/2 *100]/[(A+B+E+F)/4]

Thermal Resistance



6X Solder Shock @ 288ºCThrough hole reliability
No thin copper at the knee of the holes
No cracks nor starter cracks after 6x solder shock

Summary

- Copper Acid Process optimized to fill up a wide range of Blind Microvias
  - Minimum surface thickness
  - Optimum Fill Ratio
  - Void Free Filled BMV
- THP simultaneously
  - Mechanical Properties and Thermal Resistance meet the IPC Standards
- Results allow for enhancing via plating capabilities and increasing the reliability.

Through Via Fill

- New Technology
- Acid Copper Plating for HDI and IC Substrates
- Modifying the Copper Plating Process to accommodate the requirements for Through Hole Fill

Benefits of Through Via Hole Fill

Comparison with Conventional Hole Plugging Process (Paste)

- Improved thermal properties
- Reliability (adhesion)
- CTE
- Cost reduction
- Productivity

Through Hole Fill Process

- Differences between BMV and TH Fill processes
  - Geometric shapes
  - Hydrodynamics; solution flow in and out of the through vias
  - Center-up mechanism, as opposite to the bottom-up mechanism in case of blind micro vias

- Development work
  - Bath chemistry
  - Plating Conditions

Tests Vehicles

- Substrate Thickness 50 μm
  Through Hole Diameter 50 and 100 μm

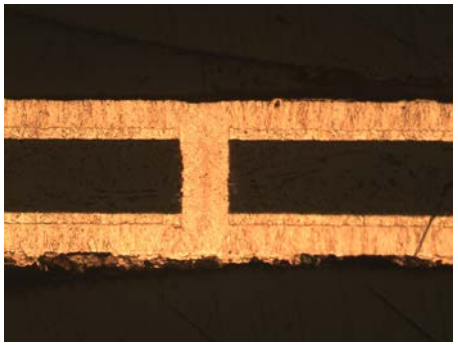
- Substrate Thickness 150 μm
  Through Hole Diameter 75, 100, 125, 150 μm

- Substrate Thickness 400 μm
  Through Hole Diameter 200 μm

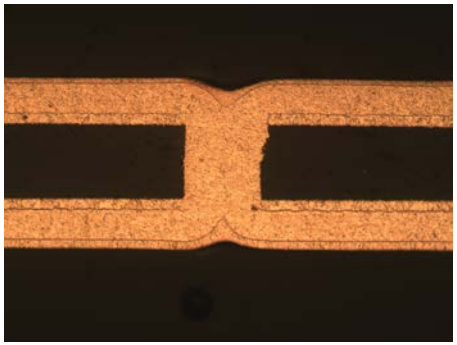
Process Parameters

- Rectification
  - Direct Current, Current density 10 -20 ASF
  - PPR
- Anodes
  - Soluble / Insoluble
- Agitation
  - Air or Eductors
- Bath Control
  - CVS Analysis, Hull cell

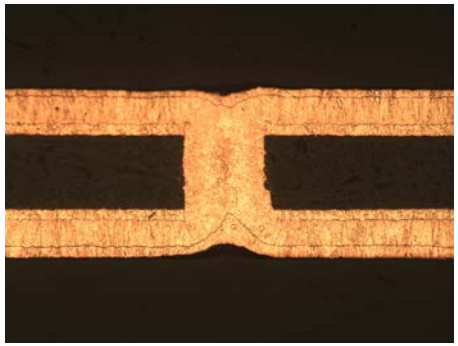
Plating Results



75 μm



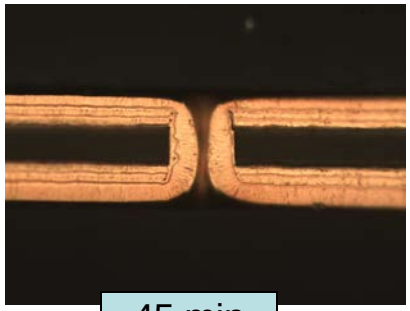
100 μm



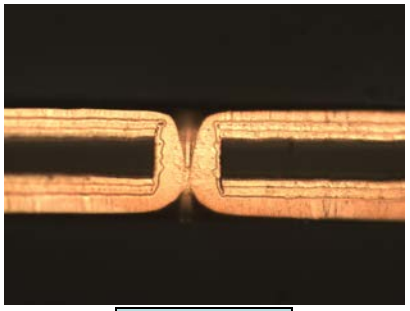
125 μm

Through Hole Fill of 150 μm thick substrate

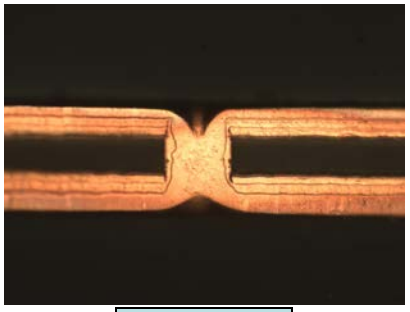
THF as a Function of Time



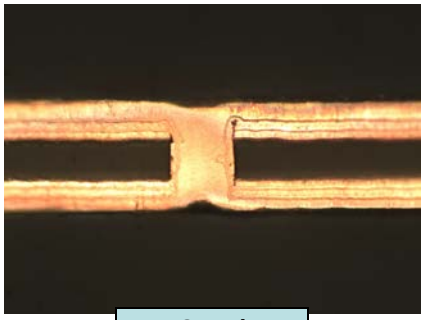
45 min



50 min



60 min

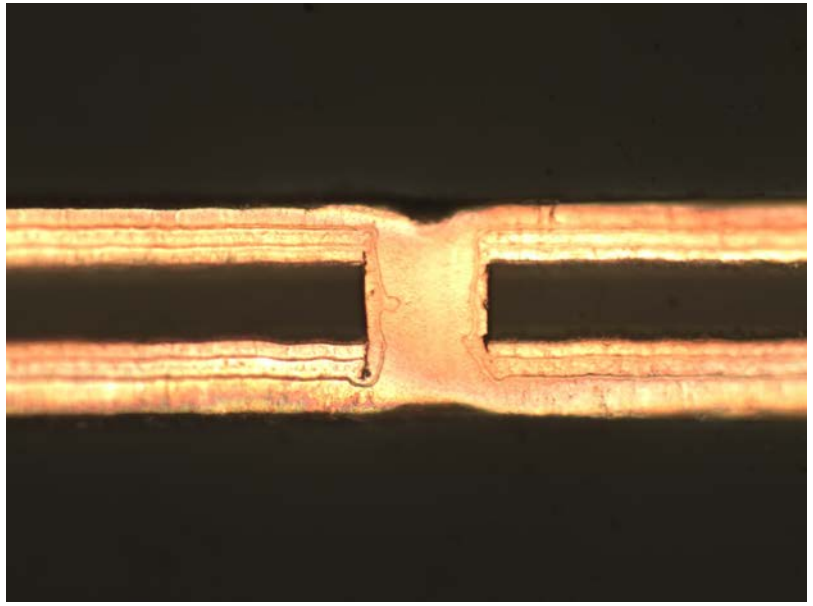


70 min

50 μm thick
x 50 μm diameter

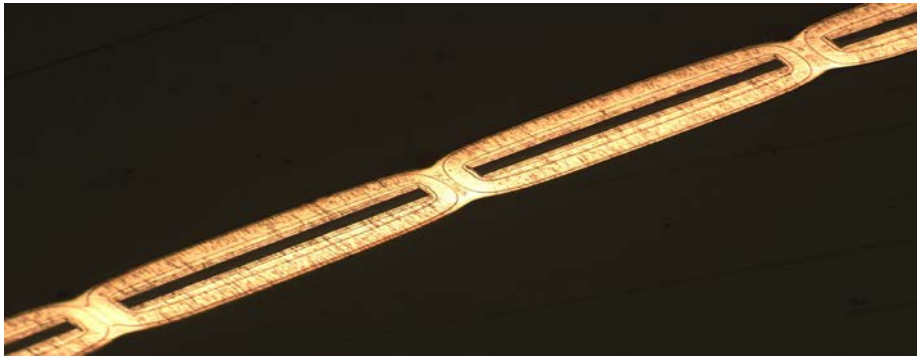
DC Plating

THF

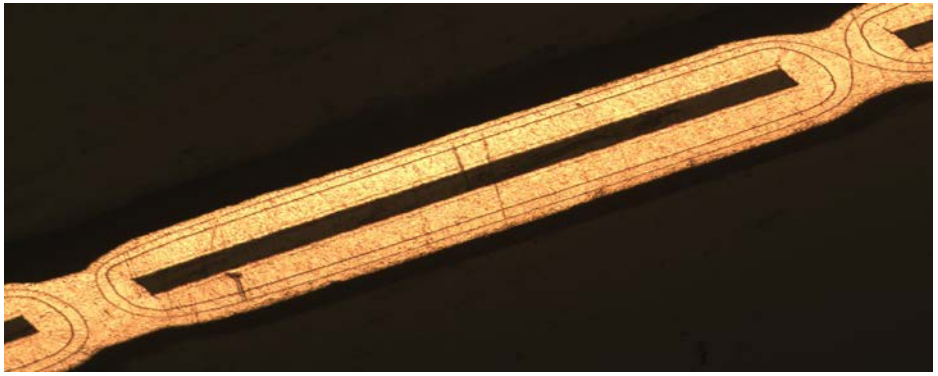


50 μm thick x 50 μm diameter

THF



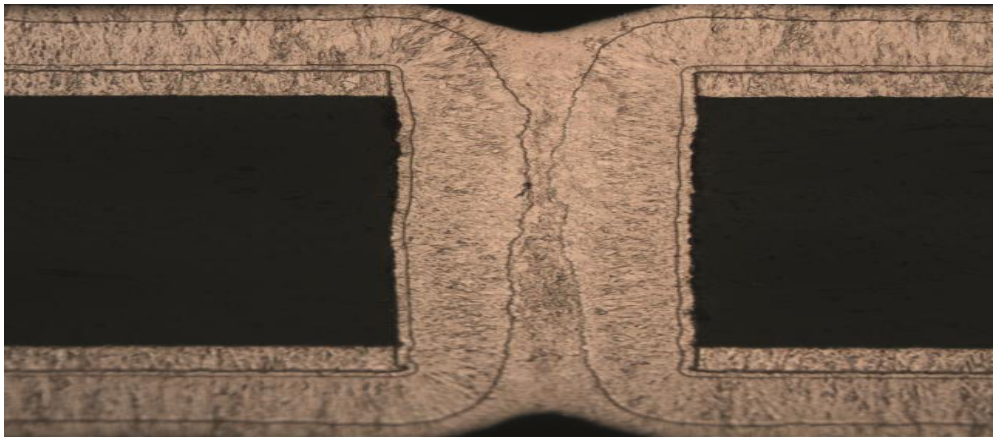
100x



200x

50 μm thick
x 100 μm diameter

THF Results



400 μm thick
x 200 μm diameter

Summary

- Through Holes geometries can be completely filed with solid electroplated copper using a modified process
- This innovative technology is at an early stage
- Further optimization will enable a variety of HDI and IC substrate package designs